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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,269	09/09/2003	Mineo Shimotsusa	03500.016072.1	3285

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EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/657,269	SHIMOTSUSA ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22,24-26 and 52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22,24,25 and 52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 22, 24, 25, 26, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination of Choi (US 6,025,237) and Richards, Jr. et al. (US patent 5,786,620) (a newly cited reference).

With respect to claims 22 and 26, AAPA teaches a method for manufacturing a semiconductor device which an electro-thermal conversion element and a switching or driving or device or insulated gate type field effect transistors for driving or flowing electric current through said the electro-thermal conversion element are integrated in a first conductive type (p) semiconductor substrate. See the Related Background Art pages 1-4 and fig. 38 of this application.

However, AAPA fails to teach the steps for forming the switching or driving element as recited in present claim 22.

Choi teaches forming a switch device comprising of (see figs. 1-13 and associated text):

forming a second conductive type (n) first semiconductor region 14 on one principal surface of a semiconductor substrate 12;

forming a gate insulator 28 on said first semiconductor region;

forming a first gate electrode 26a,b on said gate insulator;

doping a first conductive type impurity (p) by utilizing said gate electrode as a mask;

forming a second semiconductor region 20a for providing a channel region of insulated gate type field effect transistor by diffusing said first conductive type impurity; and

forming a second conductive type (n) source region 16 on the surface side of said semiconductor region by utilizing said first gate electrode as a mask such that the source region extends from beneath said first gate electrode to beneath a second gate electrode formed on said gate insulator film and a second conductive type (n) drain regions 18 on the surface side of said second conductive type (n) first semiconductor region.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the switch device as taught by Choi in the process of AAPA to obtain a switch device having high withstand voltage and low on-state resistance. See col. 3, lines 40-50.

Further with respect to claim 22, Choi teaches forming the source by ion implantation (see fig. 11) but fails to teach the implantation is performed at a titled angle.

Richards et al. teach forming a source or drain by implantation at a titled angle to extend the source under a gate. See claim 28.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Richards et al. into the process of AAPA and Choi to attain high performance device or operation. See col. 6, lines 50-55.

Further with respect to claim 26, Choi further teaches said drain region are provided in plurality 18a,b and AAPA teach connecting the drain of switching or

driving device to the electro-thermal conversion device. Choi teaches the sources are provided in plurality 16a,b are commonly connected. See fig. 1.

Further with respect to claim 22, AAPA fails to teach forming a plurality of electro-thermal conversion elements and a plurality of switching or driving devices on the same substrate.

However, It would have been obvious to one of ordinary skill in the art of making semiconductor devices to a plurality of electro-thermal conversion elements and a plurality of switching or driving devices on the same substrate to increase the number of devices on single substrate.

With respect to claim 52, Choi further teaches the drain region 18a,b is formed separated from an end of said gate electrode. See fig. 1.

With respect to claims 24 and 25, Choi further teaches performing a first conductive type ion implantation through an area between said first and second gate electrodes into at least a channel region 20a put between said source region 16 and said first semiconductor region 14 on the surface side of said second semiconductor region through said gate electrode after said step of forming said second semiconductor region and performing heat treatment for activating implanted impurity electrically. See figs. 1-13 and associated text.

Further with respect to claim 25, Choi fails to teach the use of boron and the range for implantation energy.

However, the use of boron is well-known and the range for implantation energy can be determined through routine optimization.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP